FETSIM USER'S MANUAL

AND

EXAMPLE

August 1978

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FETSIM USER'S MANUAL

GENERAL DESCRIPTION

FETSIM is a batch program written in FORTRAN IV which does D. C. and transient analysis of MOS circuits. Circuits employing N-MOS transistors and/or P-MOS transistors in either a bulk technology or an SOS technology, or almost any combination of R-C elements may be analyzed. The program requires as input data the complete circuit topology, device parameters, process parameters, and control parameters. The user can specify initial node conditions and the input pulse format. For example, pulse rise time, fall time, width and time between succeeding pulses are all independently controllable.

The program contains a sophisticated mathematical model that can accurately handle either N-MOS, P-MOS, Bulk or SOS devices. Sensitivity to process changes is maintained by requiring such process parameters as threshold voltage and doping level as program inputs. Intrinsic MOS phenomenon such as parasitic feedback capacitance and variation of threshold voltage with source potential are handled implicitly by the model. The program transforms the input data into a set of n nodal equations. These n ordinary differential equations are then numberically integrated. The output consists of a listing of n node voltages (in volts) and all transistor currents (in mA) vs time (in seconds).

The present version is dimensioned such that the program can accommodate circuits whose parameters do not exceed the following maximums:

19 nodes

5 input pulses

100 branches

50 resistors

50 capacitors

20 N-MOS transistors

20 P-MOS transistors

These limits can be expanded simply by changing the size of the appropriate valuables and arrays. Circuits having about 50 nodes require about 180,000 bytes or 45,000 four-byte words.

A user's flowchart for FETSIM is given in Fig. 1. A circuit diagram and its associated FETSIM printout are also provided as an example.

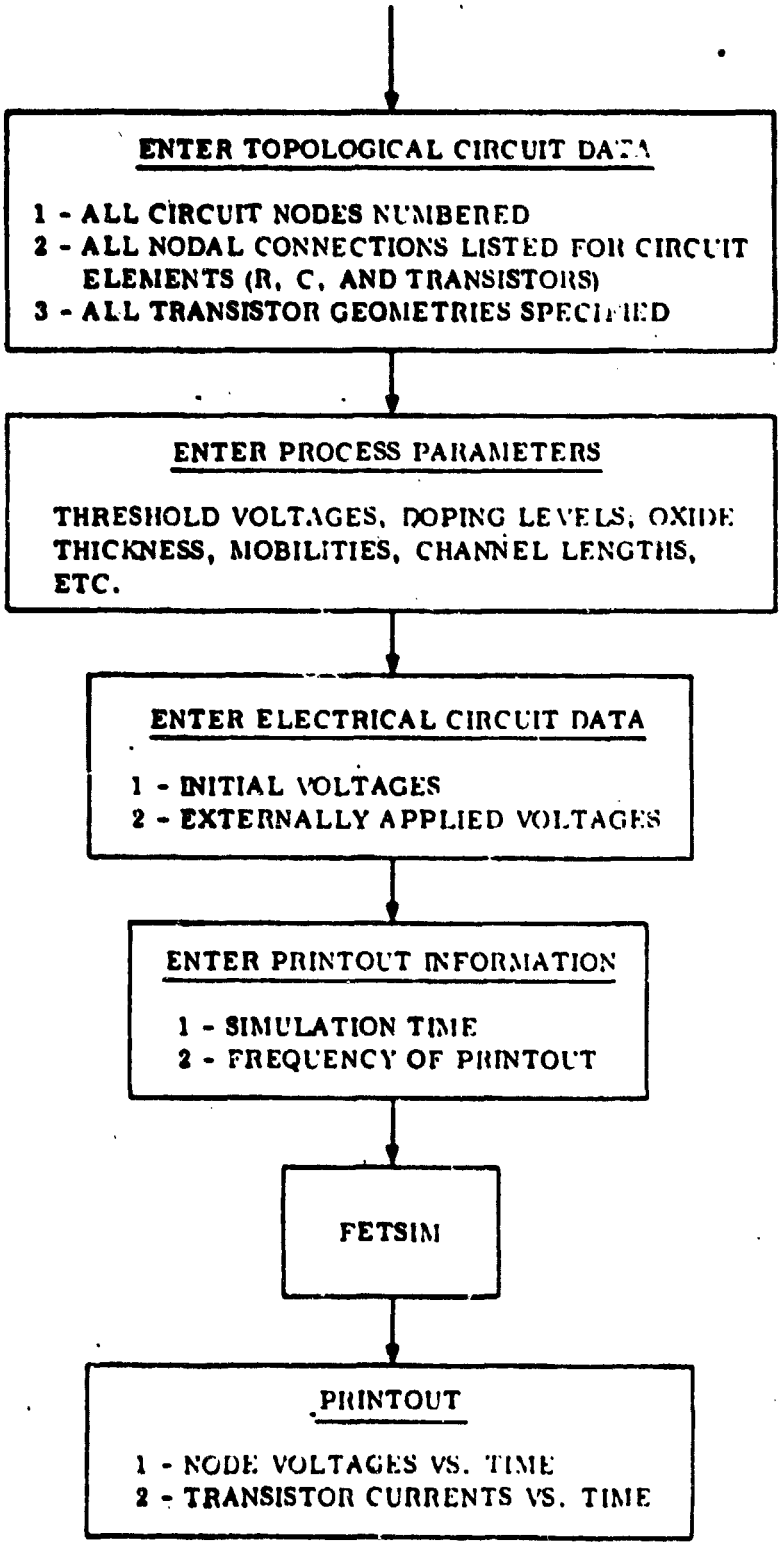


Fig. 1 FETSIM Flowchart

INPUT DATA PREPARATION

Circuit analysis begins with a schematic diagram prepared in the following way.

Number the nodes sequentially, beginning with all independent nodes. Because the program automatically connects all P-MOS substrates to node 1 and all N-MOS substrates to node 2,

NODE 1 MUST BE THE MOST POSITIVE VOLTAGE AND

NODE 2 MUST BE THE MOST NEGATIVE VOLTAGE.

Number all component types sequentially. For P-MOS transistors P(1) to P(NP), for N-MOS transistors N(1) to N(NN), for resistors R(1) to R(NR) and for capacitors C(1) to C(NC). RESISTORS AND CAPACITORS MUST BE ENTERED AS LUMPED CONSTANTS.

EVERY DEPENDENT NODE MUST HAVE A CAPACITOR CONNECTED TO IT.

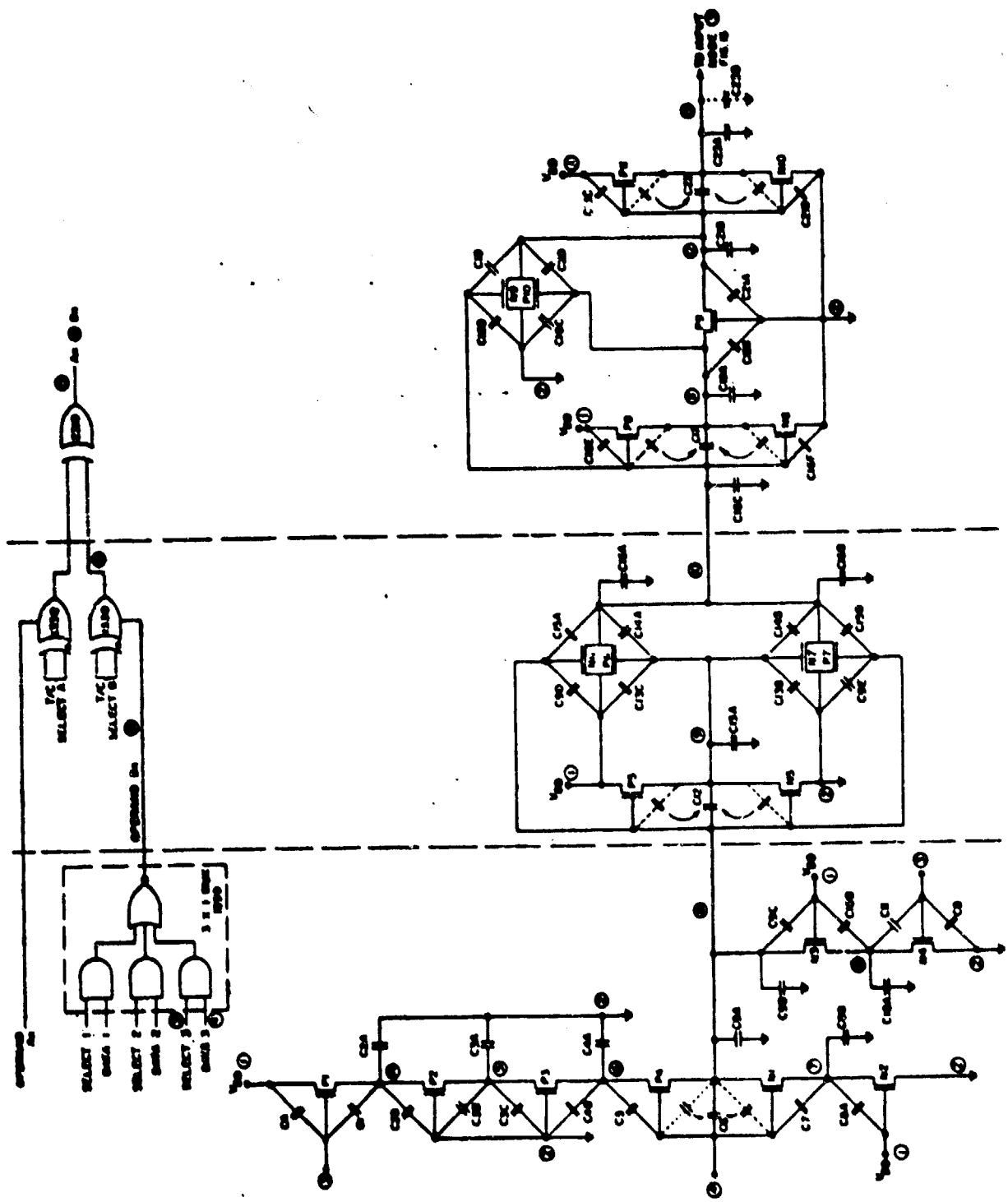


Fig. 2 Data Path 1-Logic and Circuit Diagram

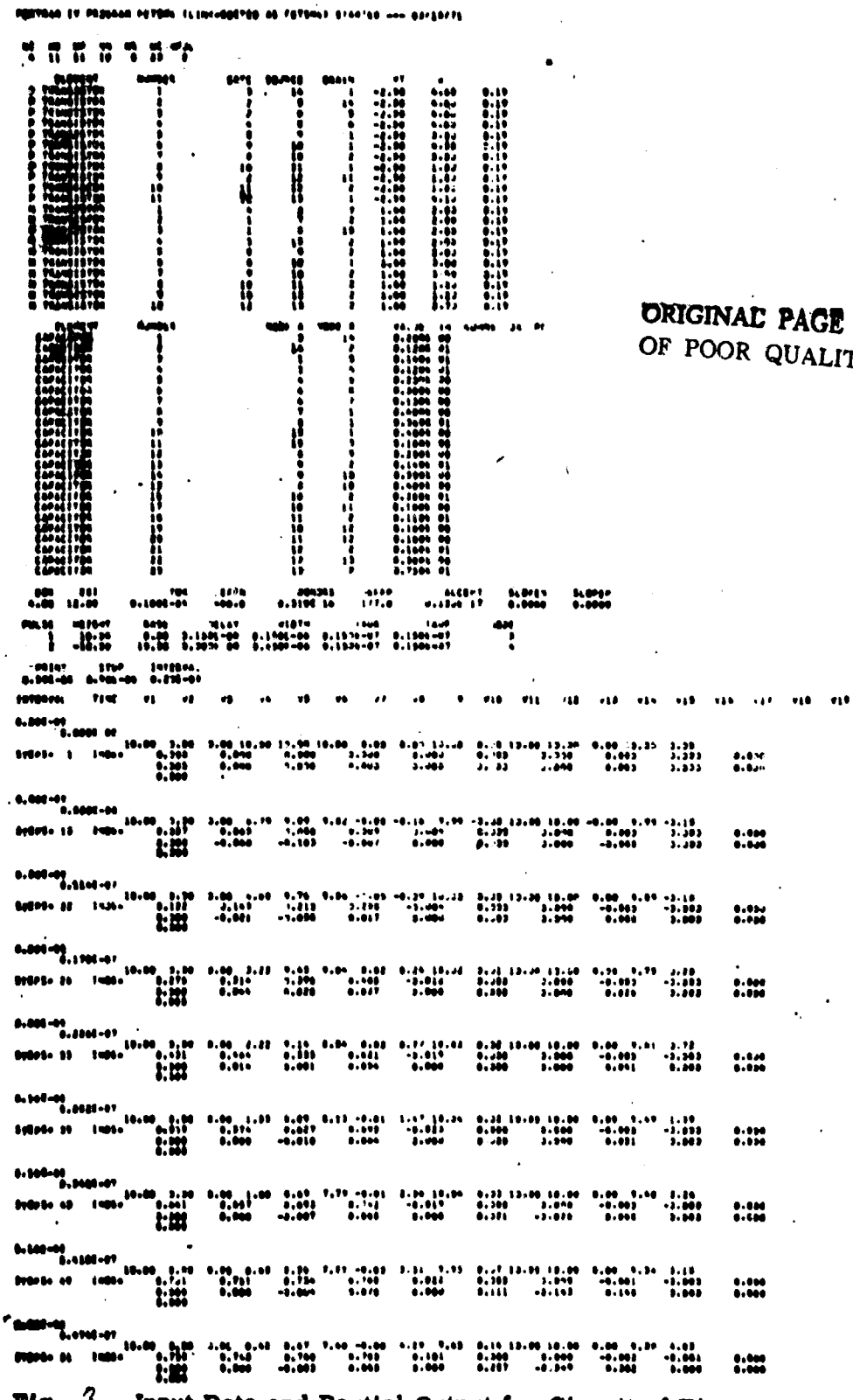


Fig. 3 Input Data and Partial Output for Circuit of Fig.

INPUT DATA IS FED INTO THE PROGRAM AS FORMATTED DATA CARDS. THE CARD SEQUENCE AND DATA ARRANGEMENT IS AS FOLLOWS:

CARD NO.	SYMBOL	DESCRIPTION	FIELD COLUMNS	FORMAT	REMARKS
1	NR	Total No. of Resistors	1-4	I	Right Justified
	NC	Total No. of Capacitors	5-8	I	Right Justified
	NP+NN	Total No. of Transistors	9-12	I	Right Justified
	NP	Total No. of P-MOS Transistors	13-16	I	Right Justified
	NI	No. of Independent Nodes	17-20	I	Right Justified
	NI+ND	Total Number of Nodes (Independent + Dependent)	21-24	I	Right Justified
	NPUL	No. of Applied Pulses	25-28	I	Right Justified
	SOS	SOS = 1 for SOS circuits; leave blank for non SOS circuits.	29-32	I	Right Justified

CARD NO.	SYMBOL	DESCRIPTION	FIELD COLUMNS	FORMAT	REMARKS
2 to (1+Np+Nn)	GATE	Gate Node No. of n^{th} Transistor	1-4	I	Right Justified, P-MOS Transistors are listed first. One Trans. is described per card. After each P-MOS Trans. has been listed, list each N-MOS Trans. on a new card.
	DRAIN	Drain Node No. Of n^{th} Transistor	5-8	I	Right Justified Source and drain nodes are interchangable and need not be distinguished.
	SOURCE	Source Node No. of n^{th} Transistor	9-12	I	
	VT	Threshold Voltage of n^{th} Trans. (in volts)	13-21	F	Right Justified The VT for P-MOS en hancement mode devices is a negative No. The VT for N-MOS enhancement mode devices is a positive NO.

CARD NO.	SYMBOL	DESCRIPTION	FIELD COLUMNS	FORMAT	REMARKS
2 to (1+NP+NN)	W	Effective channel width of n^{th} trans. (in mils)	22-30	F	Right Justified. The Nos. entered for W & L must reflect diffusion effects on mask geometries.
	L	Effective channel length of n^{th} trans. (in mils)	31-39	F	
(2+NP+NN) to (1+NP+NN +NR+NC)	TOP NODE	One node of m^{th} passive element	5-8	I	Right Justified-One Lumped constant passive element is listed on each ca
	BOTTOM NODE	Other node of m^{th} passive element	9-12	I	Right Justified Resistors if any ar listed first. Capacitors follow. Values are in KΩ and PF.
	VALUE	Value of Resistor or Cap	13-21	F	
(2+NP+NN +NR+NC)	E_{ox}	Relative permittivity of silicon dioxide	1-6	F	Right Justified. Nominal values are 4.0 & 12.0 respectively
	E_s	Relative permittivity of silicon substrate	7-12	F	Right Justified
	μ_n	Channel mobility of electrons	13-18	F	Right Justified. Mobility units are cm^2/ volt-sec
	μ_p	Channel mobility of holes	19-24	F	Right Justified
	N_D	Doping level of N-substrate	25-33	E	Right Justified. Doping level uni are atoms/cm^3
	N_A	Doping level of P-well	34-42	E	Right Justified
	T_{ox}	Gate Oxide Thickness	43-51	E	Right Justified is entered in cm. Oxide thickness units are cm. This card must be included for all FETSIM runs. Tox must always be finite.

CARD NO.	SYMBOL	DESCRIPTION	FIELD COLUMNS	FORMAT	REMARKS
↑	SLOPEN	Slope Factor for N-MOS	52-57	F	These empirical factors account for the finite positive slopes found in the saturation regions of N and P type transistors. (See Table I).
	SLOPEP	Slope Factor for P-MOS	58-63	F	
2 + NP + NN + NR + NC					
	MOVAN	Mobility Variation Factor for N-MOS	64-67	F	These empirical factors account for the effective reduction in device mobility as the gate voltage increases.
↓	MOVAP	Mobility Variation Factor for P-MOS	68-71	F	
					SLOPEN, SLOPEP, MOVAN, and MOVAP may be left unspecified by the user. In which case, an infinite saturation conductance and constant mobility are assumed.

CARD NO.	SYMBOL	DESCRIPTION	FIELD COLUMNS	FORMAT	REMARKS
↑	VH	Peak-peak voltage swing of pulse (volts)	1-7	F	Right Justified The sign of VH is positive if the pulse is positive going and negative if the pulse is negative going.
	VB	Base line of pulse (volts)	8-14	F	Right Justified
(3+NN+NP	TD	Time (in ns) that the pulse is delayed from the start of run	15-23	F	Right Justified
+NR+NC)					
	TP	Pulse width	24-32	F	Right Justified
	R	Time constant of leading edge of pulse	33-41	F	Right Justified
	F	Time constant of trailing edge of pulse	42-50	R	Right Justified
	NODE (L)	Node of circuit to which pulse is applied	51-54	I	Right Justified There may be at most five pulses. Each pulse must be described on a separate card. Al additional pulse cards follow this c
↓	TC	Time (in ns) that separates pulse A and pulse B.	55-63	F	Right justified. When this field is left blank, T_c is set to 1.0 second.

Base line
potential of
pulse -- may be
positive or nega

(the units are n

(The units are n

(The units are n

CARD NO.	SYMBOL	DESCRIPTION	FIELD COLUMNS	FORMAT	REMARKS	
(4+NN+NP	V(1)	Initial voltage at node 1	1-6	F	Right Justified	The initial conditions for node voltages V(1)---V(10) are listed on one card. In case there are more than 10 nodes, an additional card will be required For cases where there are 10 or nodes, only one card is required. (The units are volts)
+NR+NC)	V(2)	Initial voltage at node 2	7-12	F	Right Justified	
↓	V(3)	Initial voltage at node 3	13-18	F	Right Justified	
	V(4)	Initial voltage at node 4	19-24	F	Right Justified	
	V(5)	Initial voltage at node 5	25-30	F	Right Justified	
	V(6)	Initial voltage at node 6	31-36	F	Right Justified	
	V(7)	Initial voltage at node 7	37-42	F	Right Justified	
	V(8)	Initial voltage at node 8	43-48	F	Right Justified	
	V(9)	Initial voltage at node 9	49-54	F	Right Justified	
	V(10)	Initial voltage at node 10	55-60	F	Right Justified	
(5+NN+NP	V(11)	Initial voltage at node 11	1-6	F	Right Justified	An optional card to be used only when the circuit under analysis has more than 10 nodes (The units are volts)
+NR+NC)	V(12)	Initial voltage at node 12	7-12	F	Right Justified	
↓	V(13)	Initial voltage at node 13	13-18	F	Right Justified	
	V(14)	Initial voltage at node 14	19-24	F	Right Justified	
	V(15)	Initial voltage at node 15	25-30	F	Right Justified	

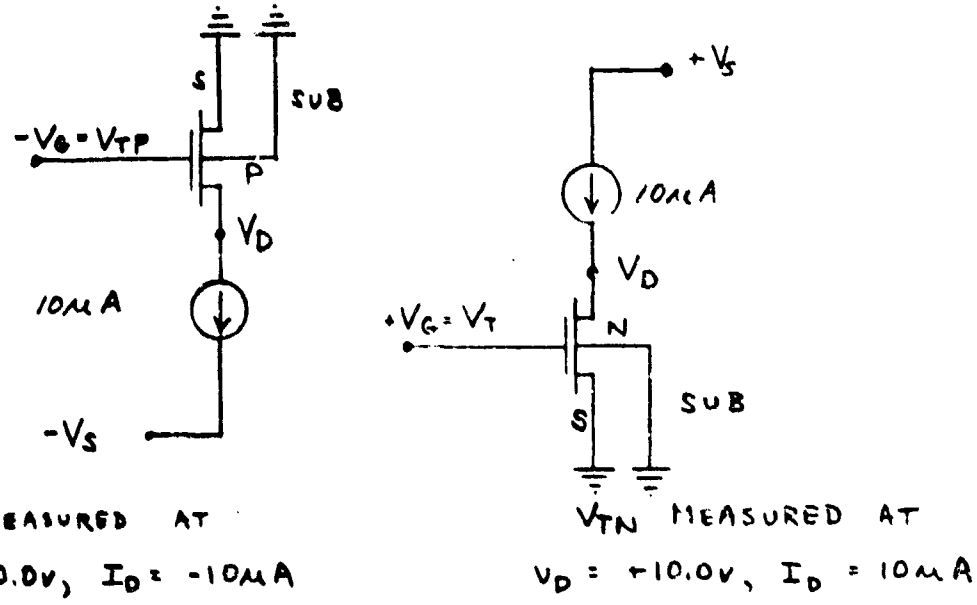
CARD NO.	SYMBOL	DESCRIPTION	FIELD COLUMNS	FORMAT	REMARKS
(5+NN+NP	V(16)	Initial Voltage at node 16	31-36	F	Right Justified
+NR+NC)	V(17)	Initial Voltage at node 17	37-42	F	Right Justified
↓	V(18)	Initial voltage at node 18	43-48	F	Right Justified
	V(19)	Initial voltage at node 19	49-54	F	Right Justified
LAST CARD	TPRINT	The time interval between print outs	1-10	E	Right Justified
↓	TSTOP	Time at which analysis stops	11-20	E	Right Justified
	INTERVAL	Initial interval of integration	21-30	E	Right Justified

An optional card to be used only when the circuit under analysis has mo than 10 nodes (The units are volts)

The units of time are entered in ns.

Threshold Voltage

For FETSIM, the threshold voltage of an MOS transistor is defined as the gate voltage required for 10 μA source-drain current with a 10 V source-drain bias. This designation is somewhat arbitrary but is widely accepted in the industry.



V_{TP} MEASURED AT
$V_D = -10.0V$, $I_D = -10\mu A$

V_{TN} MEASURED AT
$V_D = +10.0V$, $I_D = 10\mu A$

FIG 4 THRESHOLD VOLTAGE MEASUREMENT

Input Pulses

Input pulse specifications are as shown below. If T_c is left blank, the program will automatically set T_c = 1 second. In terms of 10-90% rise and fall times: $T_L = T_F = 2.2\,\tau_{L,F}$.

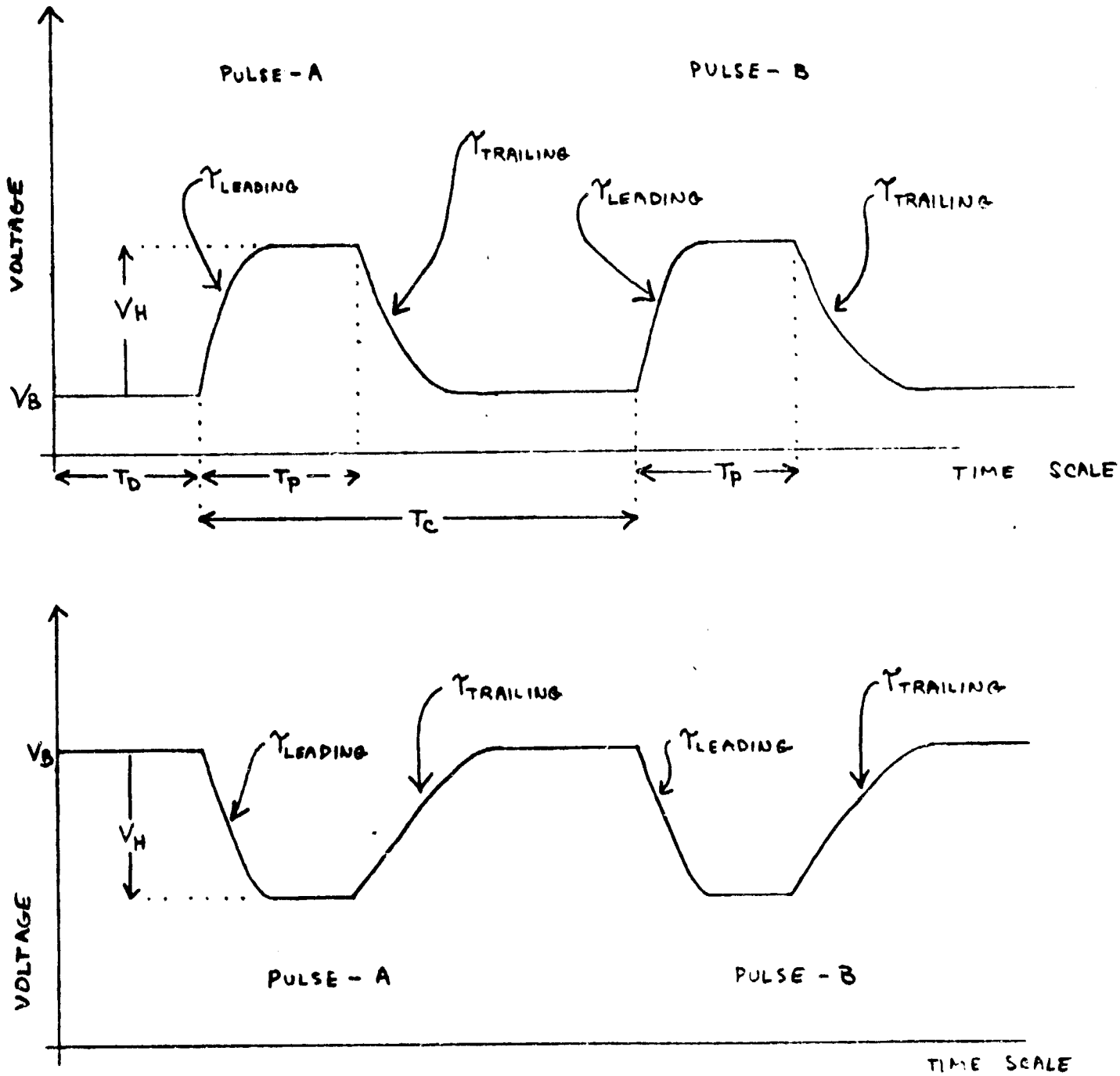


FIG 5 INPUT PULSE SPECIFICATION

FETSIM MOS MODEL

The MOS model used in FETSIM is based on a derivation following that of Ihantola.[1] By considering the doping level(s) of the ionized acceptors (or donors) in the substrate material, several second order physical effects are implicitly accounted for. These include the apparent decreased carrier mobility resulting from heavy substrate doping and the gating effect associated with stacked devices.

A linearized empirical approach[2] is utilized as a means of handling the finite drain conductances in the saturation region. In addition, surface channel mobility modulation, as a function of gate voltage, is modeled along the lines proposed by Schrieffer.[3]

The resulting four terminal MOS device model is ideally suited for large signal analysis and is directly applicable to either bulk MOS calculations or dielectrically isolated device (SOS) calculations.

Essentially the FETSIM model divides MOS transistor operation into one of three possible cases.

CASE I: $|V_G| < |V_T|$ $\qquad |V_G| < |V_{TH}|$

$$I_{DS} = \emptyset$$

Case I is the trivial case; here the magnitude of the gate voltage is below the effective threshold voltage necessary to cause transistor conduction. In this case the device current is zero.

CASE II: $|V_G| > |V_T|$

$|V_D| \leq |V_{SAT}|$

All SOS Devices or Bulk Devices when source and substrate common

$$I_D = K\left\{2V_{DS}(V_{GS}-V_T)-V_{DS}^2-4/3\,k(V_{DS}+2\emptyset F)^{3/2}\right\}$$

Case II handles the special case of a conducting transistor with its source and substrate electrically connected. The expression for the channel current contains three terms - the first two of which are those found in the generally accepted model of SAH[4]. The third term, $4/3\ \phi\ V_D^{3/2}$, introduces the effect of the substrate doping level. (The expressions for ϕ, K, V_{TH}, V_{SAT}, and α can be found in Table I.) It is this term that accounts for the reduced effective mobility associated with highly doped MOS substrates. The $(1+\alpha V_D)$ factor accounts for the finite slope of the drain characteristics in the saturation region. SOS devices are always handled with CASE I and CASE II

CASE III: $|V_{GS}| > |V_{TH}|$

$|V_D| \geq |V_{SAT}|$

$|V_S| \geq |V_{SAT}|$

All Bulk devices where source and substrate are not connected

$$I_D = K \left\{ 2(V_G - V_T)(V_D - V_S) - (V_D^2 - V_S^2) - 4/3\ k[(V_D + 2\phi F)^{3/2} - (V_S + 2\phi F)^{3/2}] \times (1 + \alpha V_{DS}) \right\}$$

Note: V_G, V_D, & V_S are measured relative to the substrate.

Case III covers the generalized and more complicated case where neither the source nor the drain are connected to the substrate. (When either the source or the drain are connected to the substrate, Case III reduces to Case II.)

Case III permits the accurate handling of "stacked" transistors (for example, 3 input NOR gates). Generally this case applies to Bulk devices only, however it is used in SOS calculations whenever device substrates are not permitted to "float".
The model is programmed in such a way as to set $V_D = V_{SAT}$ whenever $V_D \geq V_G - V_{TH}$ and $V_S = V_{SAT}$ whenever $V_S \geq V_G - V_{TH}$.

The programming technique permits saturated transistors and the gating effect to be handled.

MOS transistors processed in a bulk LSI technology share a common substrate. Generally N-MOS devices are fabricated within a common p-well while P-MOS devices are fabricated within a common n-type material. Inherent to this scheme is the possibility that the sources and drains of "stacked" transistors (in functional gates and transmission gates) can become back biased with respect to the fixed potential of the common substrates. This, "gating effect", gives rise to an apparent increase in the threshold voltages of the associated transistors. This phenomena is modeled in the equations of CASE III.

In comparison, MOS transistors processed in one of the SOS LSI technologies are fabricated, within separate, independent islands of substrate material. This technique leaves the channel material free to be defined by the source and drain

potentials of each transistor. In the case of N-MOS devices, the p-type channel material is defined by the source or drain-whichever is at the lower potential. Similarly for P-MOS devices, the n-type channel material is defined by the source or drain whichever is the higher potential. This phenomena is modeled by automatically defining the substrate of each SOS-LSI transistor to be at the lowest of the source and drain potentials for N-devices and highest of the source and drain potentials for P-devices. When this is done the more generalized CASE III reduces to CASE II.

Subroutines FET and DR contain the MOS model as described here.

TABLE I: MOS MODEL CONSTANTS

Symbol	Value	Comments
$k_{N,P}$	$\frac{T_{ox}}{E_{ox}} \sqrt{2E_S Q N_{A,D}}$	A constant which is a function of the MOS fabrication process. 'Q' is the electronic charge.
$K_{N,P}$	$\frac{u_{N,P}}{1 + MOVAN,P(V_G - V_S - V_{TN,P})} \frac{E_{ox} W}{2T_{ox} L}$	
V_{TH}	$V_T \pm k_{N,P} \sqrt{V_S + 2\phi_F}$	The sign is "+" for enhancement mode N-MOS transistors. This term accounts for the gating effect.
$\alpha_{N,P}$	Typical Values $\alpha_N = 0.01$ $\alpha_P = 0.02$	This is an empirically calculated factor which accounts for the finite slope of the drain characteristics in the saturation region.
V_{SAT}	$-2\phi_F + \left[- \frac{k}{2} + \sqrt{(\frac{k}{2})^2 + 2\phi_F + V_G - V_T} \right]^2$	
ϕ_F		The Fermi potential of the substrate.

REFERENCES

1. H. K. J. Ihantola, "Design Theory of a Surface Field Effect Transistor" Solid State Electron., Vol. 7, pp 423-430, June 1964.

2. S. R. Hofstein, Field Effect Transistors, Ed. by J. T. Wallmark and H. Johnson, Prentice-Hall, Englewood Cliffs, New Jersey, 1966.

3. J. R. Schrieffer, "Effective Carrier Mobility in Surface-Space Change Layers", Physical Review, February 1955.

4. C. T. SAH, "Characteristics of Metal-Oxide-Semiconductor Transistors," IEEE Transactions on Electron Devices, July 1964, pp. 324-325.

SOS Device and Processing Parameters

An important aspect of computer aided circuit simulation is the determination of the values of the physical device parameters. Fortunately, many of the parameters can be accurately determined from the mask layout and an elementary knowledge of the processing sequence. For a particular processing run, the parameters that are most difficult to determine are the substrate impurity concentration, N; the mobility ; the effective channel length L, the threshold voltages, VT; and the channel and field oxide thickness Tox. In the ideal case, a four terminal test transistor of known geometry will be available to provide for direct measurement of threshold voltages, drain currents, and a means of calculating the substrate impurity concentration. The mobility and effective channel lengths may also be calculated at this time, When test devices are unavailable nominal parameters may be inserted.

For most switching applications, the saturation current at full gate and drain voltage is a primary importance. It is this current (or a fixed portion of it) that will charge and discharge all load capacitors and thereby determine a circuit's dynamic performance. In a sense, it may be considered to be a composite figure of merit for all of the processing parameters. For accurate simulation results, the device saturation current predicted by the device model must therefore be equal to that measured on an actual device under identical bias conditions. For calibration purposes, the saturation current at full gate voltage is one of the parameters listed in Table II.

Table II lists the SOS parameters that are needed to both run the FETSIM program and to calculate the parasitic loading elements. The values listed are from representative samples of ATL-011 SOS test chips. Comments pertaining to the method used to arrive at these parameters are also listed.

TABLE II. SOS TEST CHIP (Ø11) DEVICE PARAMETERS

Symbol	Description	Value Used in Simulation
V_{TP}	Threshold Voltage P-Transistor (A) @ I_{DS} = 10uA	-1.5V
V_{TN}	Threshold Voltage N-Transistor (A) @ I_{DS} = 10ua	+1.5V
L	Channel Length (Effective) (B)	0.25(0.20)mils
u_p	Effective Surface Hole Mobility (V_{GS}=0) (B)	367 $cm^2/V\ s$
un	Effective Surface Electron Mobility (V_{GS}=0) (B)	458 $cm^2/V\ s$
N_D	Donor Density (C)	$1.5x10^{15}/cm^3$
N_A	Acceptor Density (C)	$1.5x10^{15}/cm^3$
T_{OX}	Gate Oxide Thickness (C)	1100A
Slope N	(In Saturation) Slope of Drain Characteristic-N (A)	0.02
Slope P	(In Saturation) Slope of Drain Characteristic-P (A)	0.01
C_{GS}	Capacitance (Gate-to-Source) (C)	$0.22p_F/mil^2$
C_{GD}	Capacitance (Gate-to-Drain) (C)	$0.22p_F/mil^2$
R_p	Resistance of Polysilicon Strip (A)	60 ohm/□
IN	Saturation Current at Full Gate and Drain Voltage (10.0V) (A)	2.3ma
Ip	Saturation Current at Full Gate and Drain Voltage (10.0V) (A)	1.6ma

(A) - obtained by direct measurement on test devices

(B) - the ratio (u/L) is chosen to adjust the simulated Saturation Current to equal the measured value. Once the ratio for each device type has been chosen, the engineer is free to chose either u or L - whichever is known to the greatest accuracy.

(C) - obtained from processing specifications

FETSIM EXAMPLE

Highlights:

1. Design/Performance review of a D-Type, S/R Flip-Flop (Standard Cell #2020).
2. Technology - double-epi, enhancement mode, SOS.
3. Processing Parameters - SOS Test Chip (ATL-011).

Summary:

The design and performance of Standard Cell #2020 is reviewed with particular attention given to evaluating output rise/fall times and clocking times. Although the actual circuit implementation incorporates 26 transistors, the analysis considers only 18 active elements. The other 8 transistors are in the Set/Reset Circuitry and have been reduced to passive elements for this analysis. The 36 parasitic capacitors (resulting from transistor gates and metal/poly/epi crossovers) and the 3 parasitic resistors (resulting from the poly and epi interconnects) are determined directly from the circuits topology (layout). The processing parameters used in the analysis are taken from samples of the Double-Epi/SOS Test Chip (ATL-011) and are listed in Table I.

The circuitry is exercised by applying waveforms to the Data and Clock inputs and observing the circuits internal and output node responses to these stimuli. Figure 1 is a detailed working schematic of the Data and Clock portions of the 2020 cell. Each node is numbered as a means of describing the circuits interconnection to FETSIM. Rise/fall times of the input waveforms are

set at 10ns (2.2x4.5ns) while the output rise/fall times may be determined directly from the printout. The loading at the Q and $\overline{Q}$ outputs is set at 10pF and 40pF respectively. Figures 2 and 3 are reduced copies of a portion of the FETSIM printout for this particular run. Figure 4 is a sketch of some of the I/O waveforms associated with this run. As can be seen a load of 4pF at $\overline{Q}$ will result in a clocked delay of 12.5ns from the falling edge of "C" to the rising edge of $\overline{Q}$. This is reflected in the 2020 cells data sheet - as can be seen in Fig. 5.

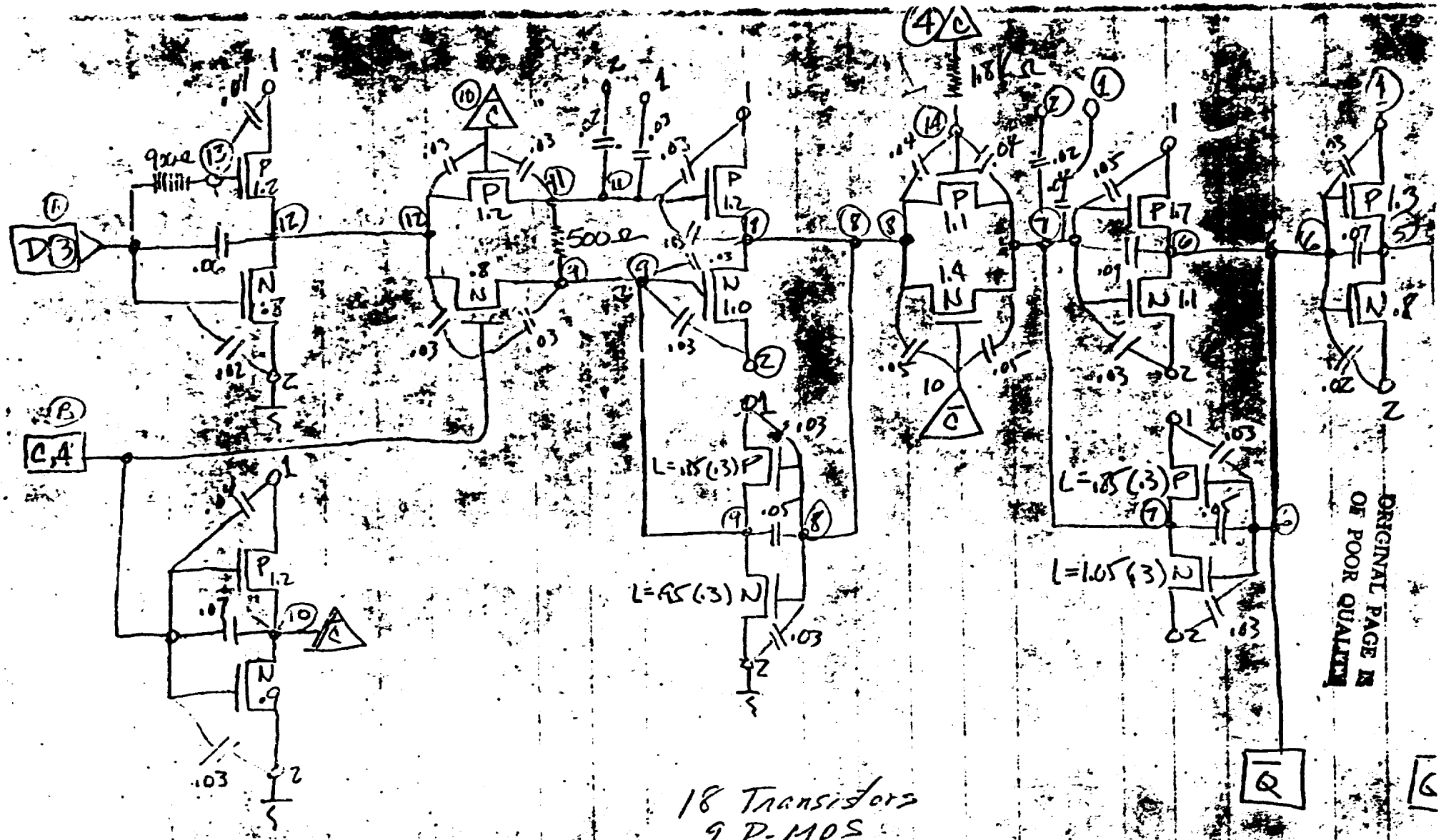

D
C
A
B
Q
500Ω
L=.18(3)P
L=.45(3)N
L=1.05(3)N
L=.18(3)P
18 Transistors
9 P-MOS
36 Caps
5 Resistors
4 Ind. Nodes
Cell = 2020
WITHOUT SET & RESET
ORIGINAL PAGE IS OF POOR QUALITY

FIG. 1

FORTRAN IV PROGRAM FETCH4 (LINK-EDITED AS FETCH4) STARTED --- 11/13/74

RESISTORS	CAPACITORS	N TRANS	P TRANS	IND NODES	TOT NODES	PULSES	SOS
3	36	9	9	4	14	2	1

ELEMENT	NUMBER	GATE	DRAIN	SOURCE	VT	W	L
P TRANSISTOR	1	13	1	12	-1.50	1.20	0.20
P TRANSISTOR	2	10	12	11	-1.50	1.20	0.20
P TRANSISTOR	3	11	1	8	-1.50	1.20	0.20
P TRANSISTOR	4	14	8	7	-1.50	1.10	0.20
P TRANSISTOR	5	7	1	6	-1.50	1.70	0.20
P TRANSISTOR	6	6	1	5	-1.50	1.30	0.20
P TRANSISTOR	7	6	1	7	-1.50	0.30	0.85
P TRANSISTOR	8	8	1	9	-1.50	0.30	0.85
P TRANSISTOR	9	4	1	10	-1.50	1.20	0.20
N TRANSISTOR	1	3	12	2	1.50	0.80	0.20
N TRANSISTOR	2	4	12	10	1.50	0.80	0.20
N TRANSISTOR	3	9	8	2	1.50	1.00	0.20
N TRANSISTOR	4	10	8	7	1.50	1.40	0.20
N TRANSISTOR	5	7	8	2	1.50	1.10	0.20
N TRANSISTOR	6	6	9	2	1.50	0.80	0.20
N TRANSISTOR	7	6	7	2	1.50	0.30	1.05
N TRANSISTOR	8	8	9	2	1.50	0.30	0.95
N TRANSISTOR	9	4	10	12	1.50	0.90	0.20

ELEMENT	NUMBER	NODE A	NODE B	VALUE IN KOHMS OR PF
RESISTOR	1	13	3	0.900E 00
RESISTOR	2	14	4	0.180E 01
RESISTOR	3	11	9	0.500E 00
CAPACITOR	1	1	13	0.400E-01
CAPACITOR	2	12	3	0.600E-01
CAPACITOR	3	9	2	0.200E-01
CAPACITOR	4	1	4	0.400E-01
CAPACITOR	5	10	4	0.700E-01
CAPACITOR	6	4	2	0.300E-01
CAPACITOR	7	12	10	0.300E-01
CAPACITOR	8	11	10	0.300E-01
CAPACITOR	9	12	4	0.300E-01
CAPACITOR	10	4	9	0.300E-01
CAPACITOR	11	1	11	0.300E-01
CAPACITOR	12	11	8	0.300E-01
CAPACITOR	13	8	9	0.300E-01
CAPACITOR	14	9	2	0.300E-01
CAPACITOR	15	1	8	0.300E-01
CAPACITOR	16	9	8	0.500E-01
CAPACITOR	17	8	2	0.300E-01
CAPACITOR	18	14	8	0.400E-01
CAPACITOR	19	14	7	0.400E-01
CAPACITOR	20	10	8	0.500E-01
CAPACITOR	21	10	7	0.500E-01
CAPACITOR	22	1	7	0.500E-01
CAPACITOR	23	6	7	0.900E-01
CAPACITOR	24	7	2	0.300E-01
CAPACITOR	25	1	6	0.300E-01
CAPACITOR	26	10	7	0.500E-01
CAPACITOR	27	9	2	0.300E-01
CAPACITOR	28	1	6	0.300E-01
CAPACITOR	29	6	5	0.700E-01
CAPACITOR	30	6	2	0.200E-01
CAPACITOR	31	11	2	0.200E-01
CAPACITOR	32	11	1	0.300E-01
CAPACITOR	33	7	2	0.200E-01
CAPACITOR	34	7	1	0.400E-01
CAPACITOR	35	6	2	0.400E 01
CAPACITOR	36	9	2	0.100E 02

EOX	ESI	TOX	UEFFN	DONORS	UEFFP	ACCEPT	SLOPEN	SLOPEP	NOVAN	NOVAP
3.90	11.70	0.120E-04	500.0	0.150E 16	400.0	0.150E 16	0.0200	0.0100	0.00	0.00

Fig. 2

```
CAPACITOR      32                    7     2    0.200E-01
CAPACITOR      33                    7     2    0.200E-01
CAPACITOR      34                    3     2    0.400E-01
CAPACITOR      35                    2     2    0.400E 01
CAPACITOR      36                    5    12    0.100E 02

   EDA     ESI          TJX        UEFFN        RBNJRS       UEFFP        ACCEPT      SLOPEM     SLOPEP     NOVAN     NOVAP
  3.90   11.70    0.120E-04        500.0     0.190E 16       400.0     0.190E 16      0.0200     0.0100      0.00      0.00

 PULSE   HEIGHT      BASE        DELAY        WIDTH        TAU LD       TAU TR        NODE       CYCLE
     1   -10.00      0.00    0.500E-07    0.200E-06    0.450E-08    0.450E-08           3    0.400E-06
     2   -10.00     10.00    0.350E-06    0.200E-06    0.450E-08    0.450E-08           4    0.400E-06

   PRINT       STOP      INTERVAL
0.40E-08    0.20E-06    0.10E-09

INTERVAL
0.10E-09    TIME
          0.000E 00    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS=  1   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.10E-08    TIME
          0.460E-08    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS= 10   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.32E-08    TIME
          0.960E-08    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS= 12   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.64E-08    TIME
          0.190E-07    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS= 14   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.64E-08    TIME
          0.254E-07    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS= 15   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.13E-07    TIME
          0.382E-07    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS= 16   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.64E-08    TIME
          0.446E-07    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS= 17   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.10E-08    TIME
          0.494E-07    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   0.00  10.00  10.00   0.00  10.00   0.00  10.00   0.00  10.00  10.00   0.00  10.00
STEPS= 19   IMOS=    0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000
                     0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000  0.000

INTERVAL
0.20E-09    TIME
          0.535E-07    V1     V2     V3     V4     V5     V6     V7     V8     V9    V10    V11    V12    V13    V14    V15    V16    V17    V18    V19
                    10.00   0.00   5.41  10.00  10.00  -0.00   0.99  -0.07   9.70  -0.05   9.66   9.47   5.37  10.00
```

FIG. 3

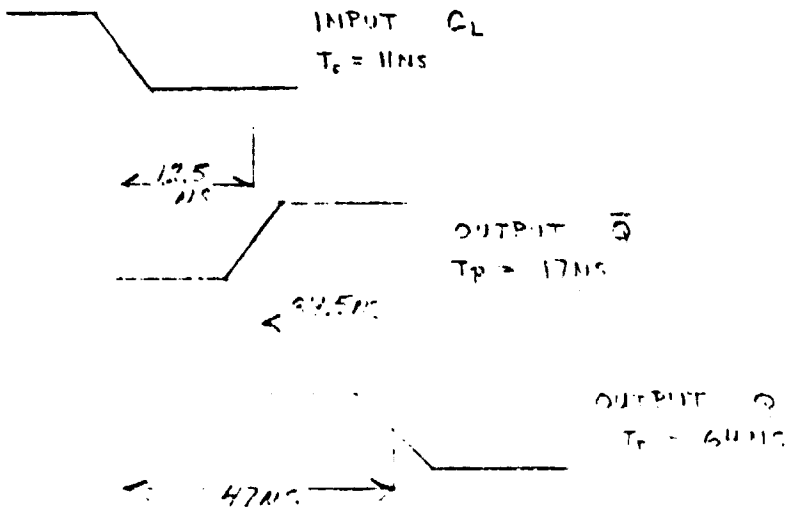


FIG. 4

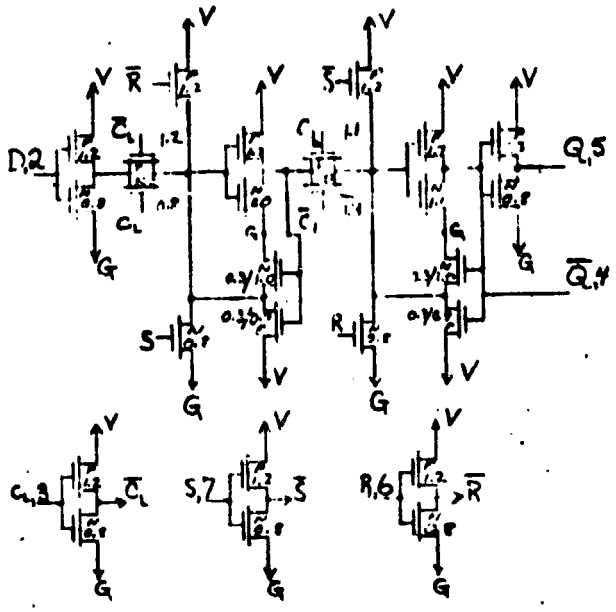
D-Type, M/S, S/R Flip Flop

SOS STANDARD
CELL NO. 2020

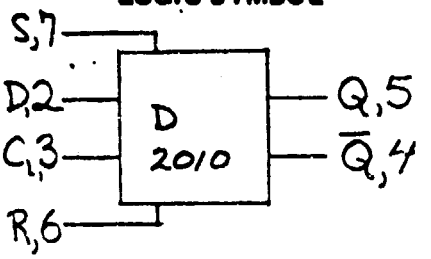
26 Devices
6 Pads

Cell Width = 14 mils

SCHEMATIC



LOGIC SYMBOL



CELL I/O CAPACITANCE VALUES

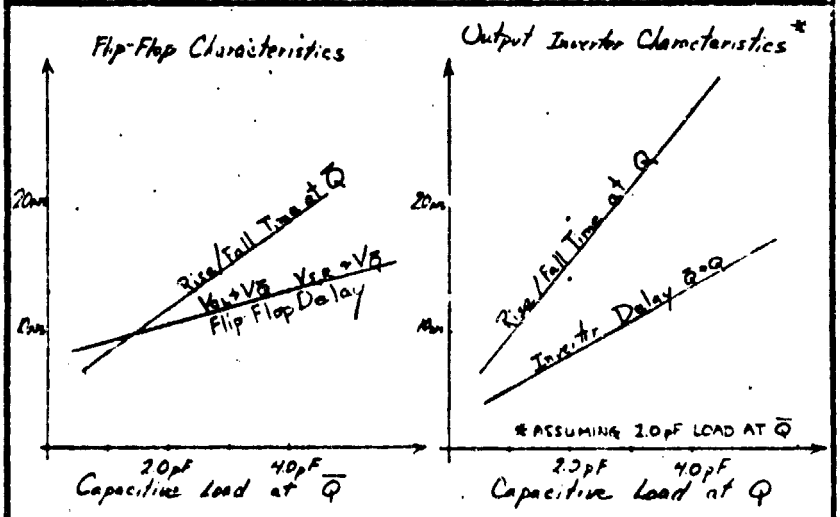
PIN	CAPACITANCE (pF)
2	0.20
3	0.42
4	—
5	0.10
6	0.20
7	0.20

TRUTH/TABLE

C_L	D	R	S	Q	$\bar{Q}$
↓	0	0	0	0	1
↓	1	0	0	1	0
*	*	1	0	0	1
*	*	0	1	1	0
*	*	1	1	✱	✱

* ~ DON'T CARE CASE
✱ ~ UNDEFINED OUTPUTS

DYNAMIC DATA



Min. Clk. to Load Master: 15NS

Min. "S" or "R" to Latch ⊕: 15NS

Min. Clk. to Load Slave: 15NS ⊕

⊕ ~ With 1.0pF at Q̄,4

TABLE I. SOS TEST CHIP (Ø11) DEVICE PARAMETERS

Symbol	Description	Value Used in Simulation
V_{TP}	Threshold Voltage P-Transistor	-1.5V
V_{TN}	Threshold Voltage N-Transistor	+1.5V
L	Channel Length (Effective)	0.25(0.20) mils
u_p	Effective Surface Hole Mobility (VGS=0)	400 $cm^2/V\ s$
u_n	Effective Surface Electron Mobility (VGS=0)	500 $cm^2/V\ s$
N_D	Donor Density	$1.5x10^{15}/cm^3$
N_A	Acceptor Density	$1.5x10^{15}/cm^3$
T_{OX}	Gate Oxide Thickness	1200 Å
Slope N	(In Saturation)Slope of Drain Characteristic-N	0.02
Slope P	(In Saturation)Slope of Drain Characteristic-P	0.01
C_{GS}	Capacitance (Gate-to-Source)	$0.2pF/mil^2$
C_{GD}	Capacitance (Gate-to-Drain)	$0.2pF/mil^2$
R_P	Resistance of Polysilicon Strip	60 ohm/

APPENDIX A

The following appendix describes the use of the graphics output capability which has been added to FETSIM. This capability is not presently supported by the Marshall Space Flight Center due to the requirement of several CALCOMP subroutines which are not presently available on the MSFC computer aided design system. These subroutines are by name:

AXIS PLOTS PLOT SCALE LINE NEWPEN

The FETSIM source tape available from MSFC has dummy routines in place of these subroutines to facilitate compilation and loading. Other functions of FETSIM are not affected by these additions.

NOT FETSIM4

ALT TAPE = 1984

FETSIM USER'S MANUAL

Appendix for Graphic Output Capability

The version of FETSIM which provides a graphic output capability is called FETGM4. FETGM4 is identical to FETSM4 with the exception of the graphic output capability.

Through the use of additional control cards, the user is able to specify the following options:

1. no graphic output
2. graphic output on only the Spectra 70 computer
3. graphic output on only the Calcomp 7000 series plotter
4. graphic output on both the Spectra 70 and the Calcomp

The additional control cards follow the FETSIM input data cards and are described below.

Control Cards

1. The first card required for the graphic output is the option control card which informs the program which of the four options previously listed is desired. The number corresponding to the desired option is placed in column 4 of the option control card. The option and their corresponding numbers are listed below:

Number	Option
0	no graphic output
1	graphic output on the Spectra 70 only
2	graphic output on the Calcomp only
3	graphic output on both the Spectra 70 and the Calcomp

2. The next card in the input sequence is the voltage selection card which specifies which node voltages are to be plotted. Since the voltages across nodes #1 and #2 are always constant, plotting of these voltages will not be allowed. The user specifies which node voltages from nodes #3 through #19 inclusive are to be plotted in columns #4 through 68 inclusive as follows:

2. (Continued)

Column No.	Node No.
4	3
8	4
12	5
.	.
.	.
68	19

If the user desires a specific node voltage to be plotted, then he places a non-zero decimal number in the appropriate column. If he doesn't want any voltages to be plotted, then a blank card must be used. The voltages will be plotted in groups of four. Automatic scaling of the voltage axis will be performed.

3. The next card in the input sequence is the trans. source current selection card which specifies which ~~branch~~ currents are to be plotted. The user specifies which branch currents from branches #1 through 40 inclusive are to be plotted in columns #2 through 80 inclusive as follows:

Column No.	Node No.
2	1
4	2
6	3
.	.
.	.
80	40

If the user desires a specific branch current to be plotted, then he places a non-zero decimal number in the appropriate column. If he doesn't want any currents to be plotted, then a blank card must be used. The currents will be plotted in groups of four. Automatic scaling of the current axis will be performed.

4. The fourth card in the input sequence is the time scaling card. This card's interpretation depends on where the graphic output is to be generated (Spectra 70 or Calcomp). For Spectra 70 output, the card specifies the number of lines per print interval . For Calcomp output, the card specifies the spacing per print interval in tenths of an inch. The allowable range is 1 to 10 inclusive. The value is specified in columns #3 and 4 and is right-justified.

If the user has specified output on either the Calcomp alone or both the Spectra and Calcomp, then the following card is required.

5. The color select option has the three general possibilities shown below:

Value	Interpretation
0	Do not stop, do not change pen
= 0	Automatically change pen at start of each current or voltage plot. Repeat pen selects.
X> 0	Stop after each X pen selects; user will change pen colors; and continue plotting. If multiple pen plotter, user may change pen colors, for example, after 4 pen selects.

The color select option is specified on its own separate card, occupies columns #3 and 4 and is right-justified.

6. If the user has specified output on either the Calcomp alone or both the Spectra and Calcomp, then he may include an additional card in his input deck which specifies the following items:

   a. the number of pens on the plotter

   b. the X-limit of the plotter

   c. the X-spacing between graphs

   d. the Y-limit of the plotter

   e. theY-spacing between graphs

   f. the Y-size of the graphs

The number of pens on the plotter is specified in column 4 and has a range of one to four. If unspecified, the default value (4) will be used.

The X-limit of the plotter is specified in columns 7 & 8 (right-justified) and has a maximum value of 72 inches. If unspecified, the default value (72) will be used.

The X-spacing between graphs is specified in column 12 and has a range of one to four inches. If unspecified, the default value (2) will be used.

The Y-limit of the plotter is specified in columns 15 & 16 (right-justified) and has a maximum value of 48 inches. If unspecified, the default value (48) will be used.

The Y-spacing between graphs is specified in column 20 and has a range of one to four inches. If unspecified, the default value (2) will be used.

The Y-size of the graphs is specified in column 24 and has a range of 6 to 9 inches. If unspecified, the default value (6) will be used.

General Operating Information

The program occupies less than 148,000 bytes of memory on the Spectra 70/45 computer and runs under control of the monitor job stream processor.

The plotting options and parameters selected by the user will be printed during the execution of the program.

Independent of where the graphs are plotted (Spectra 70 or Calcomp), each graph is limited in the time direction to a maximum of 200 time intervals (including time = 0).

If a required control card is missing or at least one of the parameters on a card is incorrect, then the message "BAD CONTROL CARD" will be printed and the program will terminate.

When the current and voltage information is being printed in tabular form on the line printer, it is also being written to the system tape called SYSUT3. When the printing of the tabular data is completed, the program rewinds SYSUT3 and reads the contents of SYSUT3 back into main memory. At this point it is possible that the program will print the message "INSUFFICIENT DATA on SYSUT3" and terminate. If this occurs, the most likely causes are either a worn tape being used for SYSUT3 or a defective tape drive.

When graphs are plotted on the Spectra 70, the four symbols used for plotting in each graph are: A, B, C, and D. If two or more symbols occupy the same position in the graph, then the symbol furthest from the beginning of the alphabet will be printed.

When output on the Calcomp plotter is requested, a standard 9-track output tape called "CALCOMP" will have to be assigned during the execution of the program. Instructions concerning the setting up of search addresses, etc. on the Calcomp plotter will be printed out on the line printer.

If the user has specified output on the Calcomp plotter, it is possible that the message "INSUFFICIENT SPACE LEFT ON THE PLOTTER" will be printed. If this occurs, it signifies that the user has not specified the X-limit and/or Y-limit on the plotter large enough to contain all of the requested graphical output.

If any suspected errors in the program arise, the user should send the output to the undersigned who will verify and correct the error.

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